

# MSOE EECS Department

## CE-1900: Lab 4 Grading Checklist

### Dr. Durant

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Name: \_\_\_\_\_

Item	Points
Homework problems	/ 20
Truth table (page 5)	/ 15
VHDL File and appropriate <b>documentation</b> per example (no deduction for format & comments, this week only) <a href="http://myweb.msoe.edu/ce1900/vhdl/hex7seg.vhd">http://myweb.msoe.edu/ce1900/vhdl/hex7seg.vhd</a>	/ 15
Simulation – include all inputs and all outputs in TT order; count through minterms in TT order	/ 10
Explanation of Simulation – <b>explain why your simulation indicates correct behavior given your design – i.e., illustrate that a few key columns give the correct output</b>	/ 15
Demonstration ( <b>individual</b> , due in lab week 5, late for partial credit)	/ 20
FAST entry (lab 3 time – lab 4 time will be checked when lab 5 is graded; see link in the Lab section on the course homepage: <a href="http://myweb.msoe.edu/durant/courses/ce1900/">http://myweb.msoe.edu/durant/courses/ce1900/</a> )	/ 5
Total	/ 100

- **Staple** this lab cover sheet on top of all the materials you are submitting.
- Submit everything in the **order** listed above.
- You may omit pages from the lab packet that do not contain work you are submitting.
- Your lab packet is due by the end of the week 5 lab period. If you are unable to complete the demonstration during the week 5 lab period, you may wish to make copies of key pages before turning in your lab packet.
- Extra copies of lab checkout sheets are available on my CE1900 website.