

MSOE EECS Department

CE-1900: Lab 6 Grading Checklist

Dr. Durant

Name: _____

Item	Points
Homework problems	/ 10
FA, VHDL, documented	/ 10
SEG7DECODE, VHDL, documented per example: http://myweb.msoe.edu/ce1900/vhdl/hex7seg.vhd	/ 15
RCA4, schematic	/ 15
LAB6, top-level schematic	/ 10
Simulation (be sure to simulate a variety of interesting values)	/ 10
Explanation of Simulation – <i>explain why your simulation indicates correct behavior given your design – e.g., illustrate that a few key columns give the correct output</i>	/ 10
Demonstration (<i>individual</i> , due in lab week 7, late for partial credit)	/ 15
FAST entry (lab 5 time – lab 6 time will be checked when lab 7 is graded; see link in the Lab section on the course homepage: http://people.msoe.edu/~durant/courses/ce1900/)	/ 5
Total	/ 100

- **Staple** this lab cover sheet on top of all the materials you are submitting.
- Submit everything in the **order** listed above.
- You may omit pages from the lab packet that do not contain work you are submitting.
- Your lab packet is due by the end of the week 7 lab period. If you are unable to complete the demonstration during the week 7 lab period, you may wish to make copies of key pages before turning in your lab packet.
- Extra copies of lab checkout sheets are available on my CE1900 website.