

MSOE EECS Department

CE-1900: Lab 8 Grading Checklist

Dr. Durant

Name: _____

Item	Points
Prelab 1: ALU BS TT	/ 7
Prelab 3: FA TT	/ 3
Prelab 3: fulladd VHDL, documented per standard (no sim)	/ 5
Prelab 3: le VHDL, documented	/ 7
Prelab 4: le simulation , show all possible input states; 4+ states for various operations illustrated and verified for correctness	/ 6
All remaining VHDL, documented: ae, ce, hex7seg	/ 13
Schematics (include your name and date in text comments): alubs, alu4	/ 10
Prelab 6: alu4 simulation – Explain why your simulation indicates correct behavior given your design. <i>I.e., confirm correct output for ALL 8 operations for nontrivial inputs (e.g., A=0011, B=0110).</i>	/ 20
Prelab 7: toplevel schematic (note: NO toplevel simulation needed this week, but, if you prefer, you may do that <i>instead</i> of the ALU4 simulation as long as the required information above is shown)	/ 4
Demonstration (-10% per (partial) day late)	/ 20
FAST entry (lab 7 time – lab 8 time will be checked when lab 9 is graded; see link in the Lab section on the course homepage: http://myweb.msoe.edu/durant/courses/ce1900/)	/ 5
Total	/ 100

- **Staple** this lab cover sheet on top of all the materials you are submitting.
- Submit everything in the **order** listed above.
- You may omit pages from the lab packet that do not contain work you are submitting.
- Your lab packet is due by the end of the week 9 lab period. If you are unable to complete the demonstration during the week 9 lab period, you may wish to make copies of key pages before turning in your lab packet.
- Extra copies of lab checkout sheets are available on my CE1900 website.