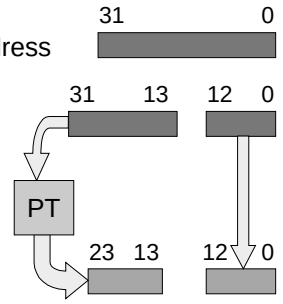
Address Translation Process

Start with virtual address

Split into page & displacement

Translate via page table

Form physical address



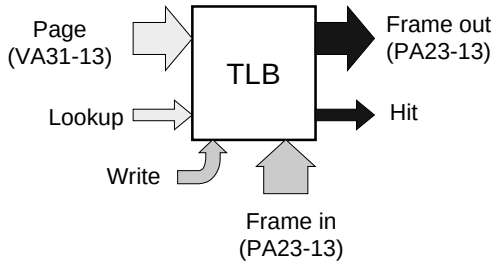
Hardware Support for Paging

- **Page table implementation**
  - Dedicated registers
    - Usually impractical due to size
  - Main memory
    - With PTBR - page table base register
- **Performance problem**
  - Long address translation time

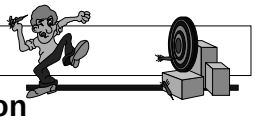
Translation Look-Aside Buffer

- **Also known as TLB**
- **Caches page table**
  - Avoid page table memory access
- **Associative memory**
  - Addressed by content, not location!
  - Reports success or failure (hit/miss)

TLB Block Diagram



TLB Design Issues



- **Memory organization**
- **Lookup technique**
- **Update (write) method**
  - Invoked on TLB miss
  - Load frame from page table
- **Speed, complexity, cost**

TLB Design Exercise

- **Assume**
  - 1024 TLB entries
  - Virtual address: 32 bits
  - Physical address: 24 bits
  - Page size: 8192 bytes
- **Design TLB hardware**