

Complete this page, but do not open the test until you are instructed to do so. You will have sixty (60) minutes to complete the exam. The exam is closed book and notes. No calculators are allowed. Make sure you budget your time well. Strategy statements are not required unless specifically requested (problems 4, 5, and 6).

Check which section you are in: 8:30 _____ or 11:30 _____

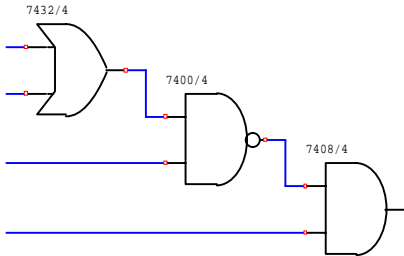
Write down your seat assignment: Row _____ Number _____

Scores:

Problem	Possible	Attained
1a	5	
1b	5	
1c	5	
1d	5	
1e	5	
1f	5	
2	10	
3	10	
4	10	
5	20	
6	<u>20</u>	<u> </u>
Total	100	

1. Each part is worth 5 points (total 30pts). There will be no partial credit on this question.
a) List all minterms possible for a two-input function, $F(X,Y)$.

- b) Convert the following circuit into a circuit consisting of NAND and NOT gates only.



- c) How many prime implicants are in the following K-map?

			W		
	1	1	0	1	
	1	1	0	1	
	0	1	1	1	Z
Y	0	0	0	1	
		X			

Answer: _____

- d) For the same K-map, clearly show the essential prime implicants.

			W		
	1	1	0	1	
	1	1	0	1	
	0	1	1	1	Z
Y	0	0	0	1	
		X			

- e) Use DeMorgan's Law to write an expression for the complement of $F = X(Y' + Z)$ in terms of AND and OR gates only. Assume that you have all the literals available to you.

- f) Rewrite the following expression in its simplest form:

$$F = (X' + Y' + Z)(X' + Y + Z)(W'XZ)'(WXZ)'$$

2. Given the following K-map

F		W				
		1	0	0	1	
Y	0	1	1	1	Z	
	0	0	0	0		
	1	0	0	1		
	X					

(4pts) a) Construct the Truth Table for F.

W	X	Y	Z	F
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	

0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	

1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	

1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

(3pts) b) Write the canonical POS form of F. (The shorthand notation is not sufficient.)

(3pts) c) Write the canonical POS form of the complement of F. (The shorthand notation is not sufficient.)

3. Design a circuit that asserts its output, F, whenever a majority of 3 inputs, X, Y, & Z, are asserted.
(3pts) a) Create the truth table.

(3pts) b) Write the minterm expansion for this circuit. (The shorthand notation is not sufficient.)

(4pts) c) Using a K-map, write the minimal sum of products expression for F.

4. Using any method prove the following relation: $YZ + XYZ' + X'Y'Z = XY + X'Z$

(4pts) a) Strategy:

(6pts) b) Solution:

5) (20pts) Suppose your instructor lost his voice. He also decided that just writing on the overhead would be as boring as a monotone voice, so he has devised the following scheme for communicating with the class. Students may ask yes/no questions. If the answer to the question is yes, your instructor will throw a piece of paper into the trash can. If the answer is no, he will throw the piece of paper onto the floor near the can. After every three answers, a fourth “parity paper” is thrown. It should land in the trash can if an even number of the first three pieces of paper should have landed in the trash. Otherwise it should land on the floor near the can. Thus, if the “parity paper” falls in the can, the first three answers (papers) are assumed correct only if an even number fell in the can. If the “parity paper” does not fall in the can, the first three papers are assumed correct only if an odd number fell in the can.

Label pieces of paper that fall in the trash can with a one and those that fall on the floor with a zero. Assume that in any collection of four tosses, at most one piece of paper misses its intended destination.

a) Design a circuit with output, F, that will produce a 1 if the answers are assumed correct.

W	X	Y	Z	F
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	

0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	

1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	

1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Write your strategy for each part here:

Strategy for a)

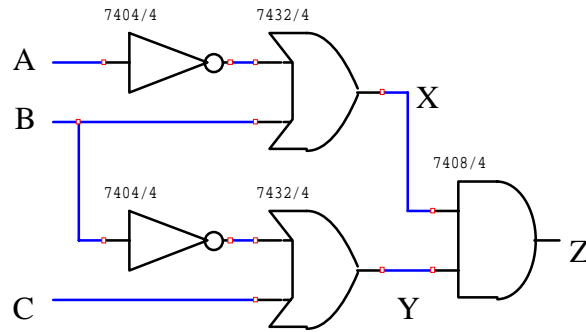
Strategy for b)

Strategy for c)

b) Construct the K-map for this function.

c) Write the minimum SOP expression from the K-map.

6) (20pts) Consider the following circuit:



a) What kind(s) of static hazards are possible for this particular circuit?

b) Identify all possible input transitions that may lead to a static hazard.

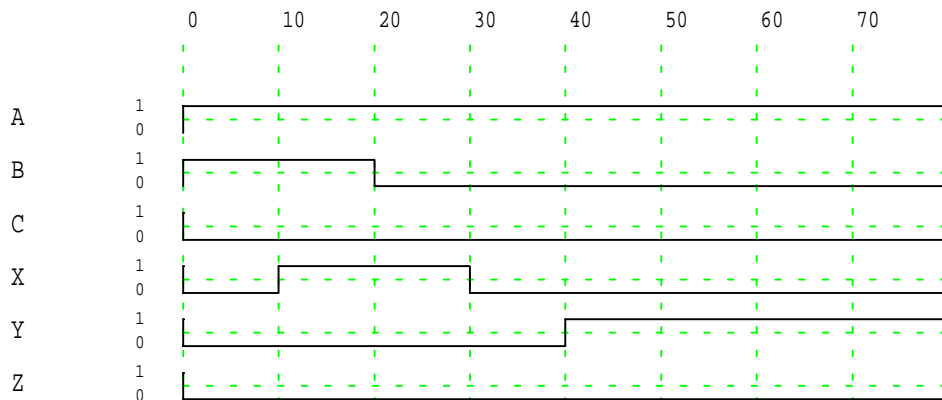
Strategy:

Solution :

c) Complete the trace assuming each gate (including inverters) has a delay of 10 time units.

Strategy:

Solution:



d) Does the transition from 110 to 100 result in a static hazard? Yes No (circle one)
If yes, identify the static hazard.