

EE 266**Exam II: March 22, 1995**

Complete this page, but do not open the test until you are instructed to do so. You will have sixty (60) minutes to complete the exam. The exam is closed book and notes. No calculators are allowed. Make sure you budget your time well. Strategy statements are not required unless specifically requested (problems 2 & 3).

Check which section you are in: 8:30 _____ or 11:30 _____

Write down your seat assignment: Row _____ Number _____

Scores:

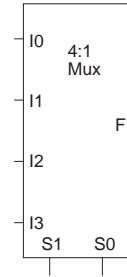
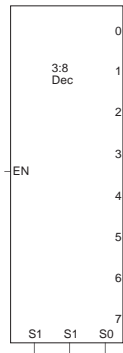
Problem	Possible	Attained
1a	9	_____
1b	6	_____
2	15	_____
3	15	_____
4	10	_____
5	10	_____
6a	2	_____
6b	4	_____
6c	4	_____
6d	5	_____
6e	5	_____
7	15	_____
Total	100	_____

1.

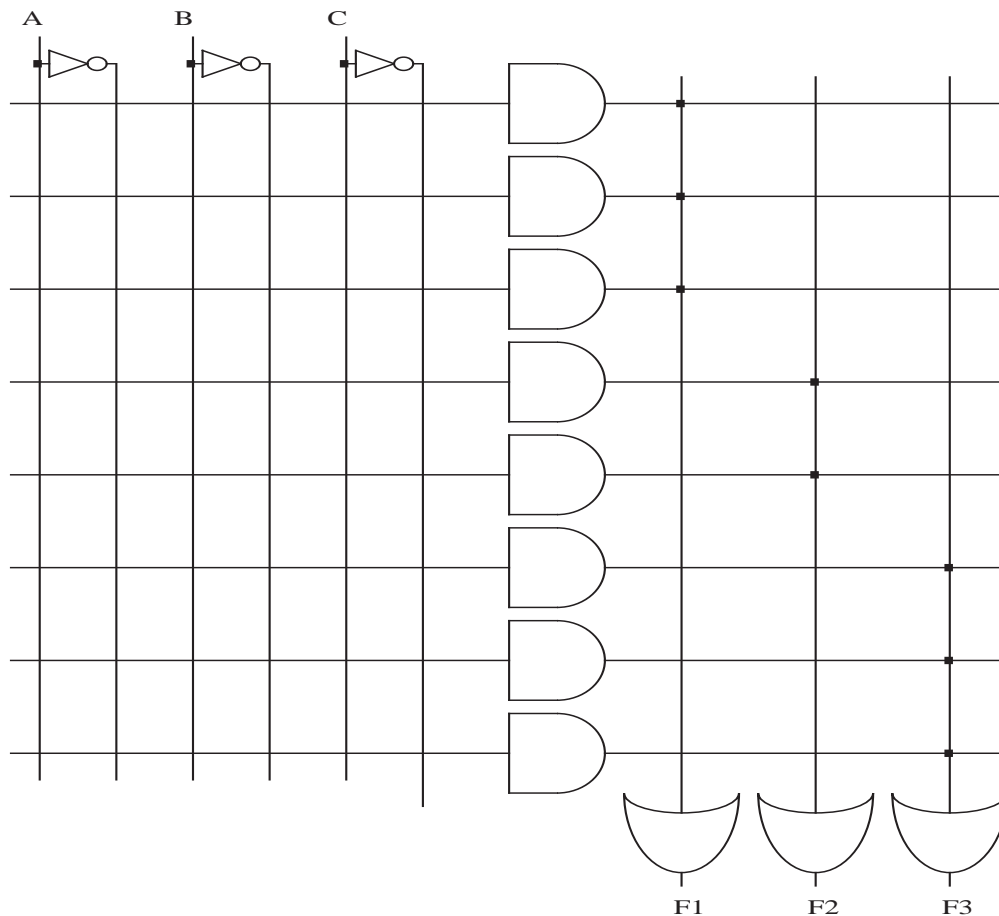
- (a) (9 pts.) Design a circuit that uses a 3:8 decoder, a 4:1 mux and OR gates of any type to implement the following functional truth table.

X_1	X_0	Y
0	0	0
0	1	F_1
1	0	F_2
1	1	F_3

where $F_1(A, B, C) = \sum m(0, 3, 7)$
 $F_2(A, B, C) = \sum m(0, 4, 7)$
 $F_3(A, B, C) = \sum m(1, 5, 6)$



- (b) (6 pts.) Implement F_1 , F_2 , and F_3 using the following PAL. Note: F_2 has only two product terms.

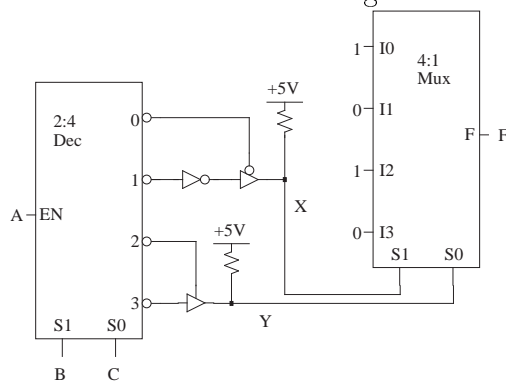


2. (15 pts.) Implement F using one 4:1 mux with $S_1 = A$, $S_0 = B$ and as few 2:1 muxes with $S_0 = C$ as possible. Assume all literals are available.

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Strategy: (4 pts.)

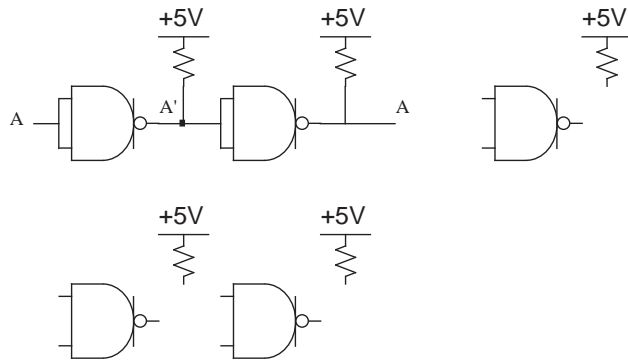
3. (15 pts.) Complete the truth table for the following circuit.



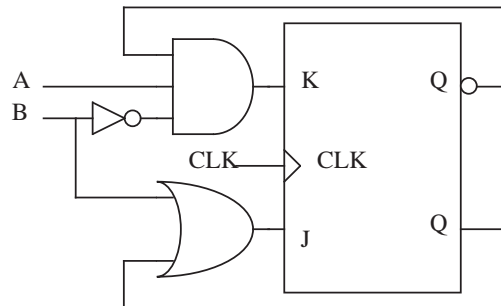
A	B	C	X	Y	F
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

Strategy: (5 pts.)

4. (10 pts.) Connect the circuit components below so that they implement the function $F(A, B, C, D) = \sum m(11, 15)$. (You may not need all the parts.)



5. (10 pts.) Find the characteristic equation for the following circuit.



6. The Adder.

- (a) (2 pts.) Write the Boolean expressions for the sum and carry-out for a full adder in terms of A_i , B_i and Carry-in C_i .

$$S_i =$$

$$C_{i+1} =$$

- (b) (4 pts.) The text defined carry propagate to be $P_i = A_i \oplus B_i$. We can also define it to be $P_i = A_i + B_i$. In this case, show that $C_{i+1} = P_i(G_i + C_i)$, **and** $S_i = (G_i'P_i) \oplus C_i$.

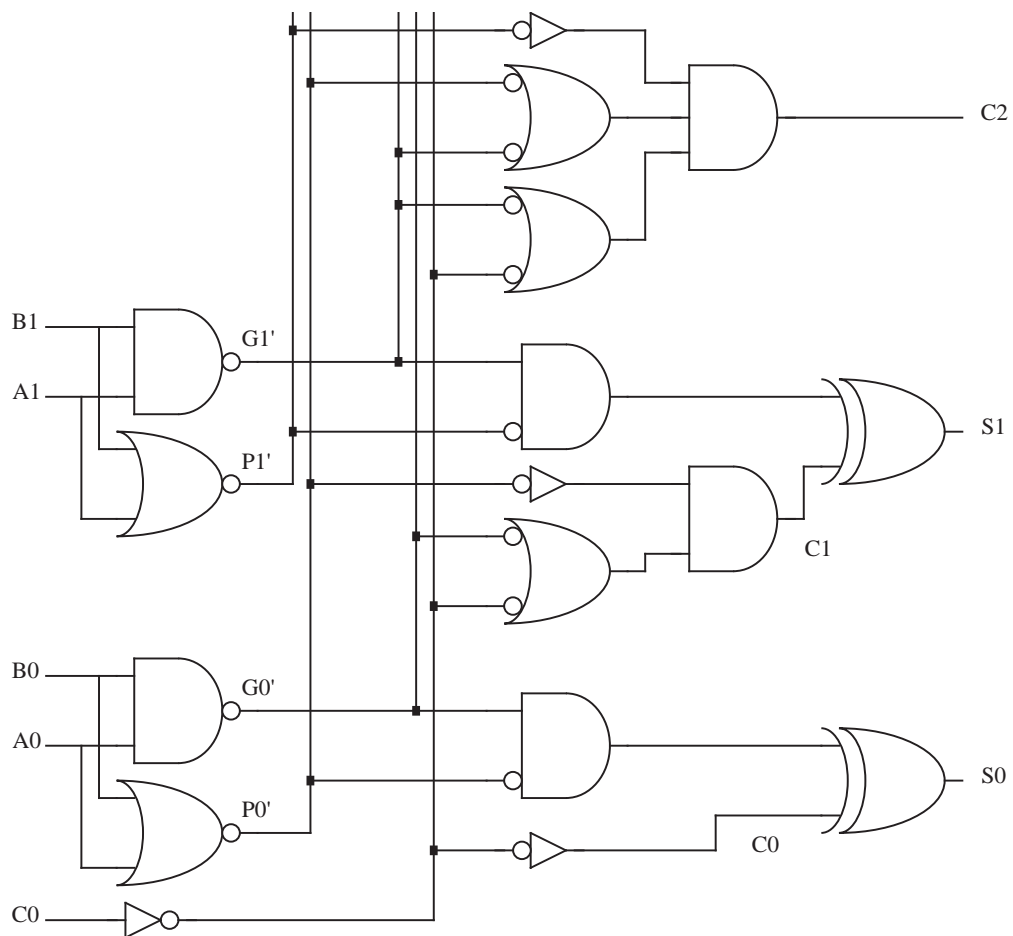
- (c) (4 pts.) Derive 2-level SOP forms for C_1 and C_2 in terms of C_0 , P_1 , G_1 , P_0 , and G_0 .

$$C_1(P_0, G_0, C_0) =$$

$$C_2(P_1, P_0, G_1, G_0, C_0) =$$

- (d) (5 pts.) Derive the minimal POS forms for C_1 and C_2 in terms of C_0 , P_1 , G_1 , P_0 , and G_0 .

- (e) (5 pts.) Show that the following circuit either does or does not implement the 2-bit adder. HINT: SEE IF S_0 , S_1 , AND C_2 AGREE WITH ANY OF THE PREVIOUS PARTS.



7. (15 pts.) Complete the timing diagram for the circuit. Assume each gate has a delay of 10 nanoseconds. NOTE: A DEPENDS ON C₁.

