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Memory Types

- Three types of storage cells
 - ◆ “Fixed” – Can’t be “changed”
 - ◆ Static – Remember by themselves
 - ◆ Dynamic – Remember with help
- Three storage issues
 - ◆ Writability – Can we change it?
 - ◆ Volatility – Does it need power to remember?
 - ◆ Speed – How slow is it?

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ROM/PROM Memory

- Read only
 - ◆ During normal operation
- Designed for non-volatility
- Used to store programs
 - ◆ Operating systems
 - ◆ Embedded software
- Programming
 - ◆ Factory mask
 - ◆ Once in-house

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UVEPROM

- Ultraviolet Erasable PROM
- Operation
 - ◆ Fusible links are selectively blown by high voltage
 - ◆ Memory is used
 - ◆ Links are mended by 20-30 minutes of high-intensity UV light
- Usage
 - ◆ Prototyping prior to ROM/PROM use
 - ◆ Systems requiring regular upgrade

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EEPROM

- Electrically Erasable PROM
 - ◆ Links/cells can be reset electrically
 - ◆ Typically slow (8.5 ms on ATmega32)
 - ◆ Often in blocks
- Compromise between RAM and UVEEPROM
 - ◆ Non-volatile, but writable
- Usage
 - ◆ Configuration information to be retained
 - ◆ Large embedded system “ROM”

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Static RAM (SRAM)

- Memory cells built around D flip-flops
 - ◆ Obvious circuit design
- Properties
 - ◆ Very fast (the fastest memory)
 - ◆ Expensive (space/bit, \$/bit)
- Usage
 - ◆ Variables in embedded systems
 - ◆ Cache memory

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Dynamic RAM (DRAM)

- Memory cells built around capacitors
 - ◆ Stored charge looks like a voltage
- Properties
 - ◆ High-density
 - ◆ Requires refresh due to charge leakage
- Common in SIMMS and DIMMS

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DRAM Refresh

- The stored charge must be reinforced
 - ◆ Periodic activation of the column address
 - ◆ Typically done during idle time
 - ◆ e.g. Decode phase
- Significant drawback
 - ◆ Custom or built-in controllers are common
- Typically too much hassle for embedded systems
 - ◆ RAM needs don't require the storage capacity

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Memory Summary

Type	Writable	Volatile	Write Speed	Comments
ROM	N	N	N/A	Factory
PROM	Y	N	Slow	Write once
UVEPROM	Y	N	Very Slow	20-30 minutes Special voltage
EEPROM	Y	N	Slow	8+ ms, Block erase Special voltage
Static RAM	Y	Y	Very fast	\$\$
Dynamic RAM	Y	Y	Fast	Refresh

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EEPROM on the ATmega32

- 1024 bytes
 - ◆ Separate address space
 - ◆ Accessible by program and external interface
- Access through special registers
- Write time is 8.5 ms
 - ◆ Also causes 2 and 4 cycle halts of the CPU

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Programming the EEPROM

Bit	7	6	5	4	3	2	1	0	
	-	-	-	-	EERIE	EEMWE	EEWE	EERE	EEDR
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	X	0	

Courtesy of ATMEL.

- EERIE – EEPROM ready to write interrupt
 - ◆ Vector \$022
- EEMWE – Master write mask (set first)
- EEWE – Start write operation
- EERE – Trigger a read

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Routine for Writing to EEPROM

```
// Wait for completion of previous write
while(EEDR & (1<<EEWE)) {}

EEAR = uiAddress; // Set address
EEDR = ucData;    // Set data

EEDR |= (1<<EEMWE); // Master write enable

EEDR |= (1<<EEWE); // Trigger write
```

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Routine for Writing to EEPROM

```
// Wait for completion of previous write
while(EEDR & (1<<EEWE)) {}

EEAR = uiAddress; // Set address

EEDR |= (1<<EERE); // Trigger read

result = EEDR; // Get the data
```
